ADTEC

PC4-3200 4GB ECC 1Rank SO-DIMM

(compatible with PC4-2933, PC4-2666, PC4-2400, PC4-2133)

Note: ADTEC Corporation reserves the right to change products and specifications without notice.

Description

This Memory Module is PC4-2400 Double Data Rate 4 (DDR4) 4GB (x72, ECC SR) 260-pin Small Outline Dual In-Line Memory Module (SO-DIMM).

Feature

- 260-pin Small Outline Dual In-Line Memory Module (SO-DIMM)
- Module Height: 30mm
- DDR4 functionality and operations supported as defined in the component data sheet
- Fast data transfer rates: PC4-3200 (compatible with PC4-2933, PC4-2666, PC4-2400, PC4-2133)
- V_{DD} = 1.20V (NOM)
- V_{PP} = 2.5V (NOM)
- V_{DDSPD} = 2.5V (NOM)
- Nominal and dynamic on-die termination (ODT) for data, strobe, and mask signals
- Low-power auto self refresh (LPASR)
- Data bus inversion (DBI) for data bus
- On-die V_{REF}DQ generation and calibration
- 16 internal banks (x4, x8): 4 groups of 4 banks each
- Fixed burst chop (BC) of 4 and burst length (BL) of 8 via the mode register set (MRS)
- Selectable BC4 or BL8 on-the-fly (OTF)
- Temperature range
  - — Operation 0℃ ≦ Tc ≦ 85℃※
    Storage -55℃ ≦ Tc ≦ 100℃

    ※Some applications require operation of the Extended Temperature Range between 85℃ and 95℃ case temperature.
    Refresh commands must be doubled in frequency, therefore reducing the refresh interval tREFI to 3.9us.

- PCB
  - — JEDEC compliant
  - — Flammability meets UL94V-0
    Material FR4
    Plating Ni= 2.00μm MIN
    Au= 0.76μm MIN
  - — Solder resist Halogen free
  - — Gold edge contacts and chamfer the corners

- Onboard I2C serial presence-detect (SPD) EEPROM

- RoHS2 compliant

DRAM

- Part Number: K4A4G085WG-BCWE
- Vendor: Samsung

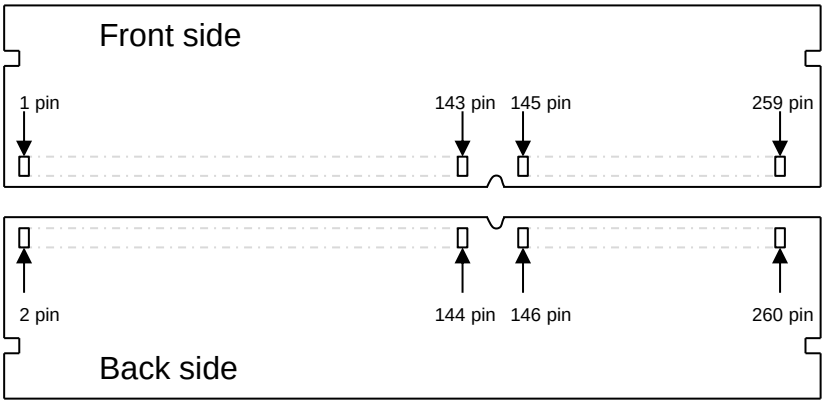
Pin Description

Symbol	Type	Description
A0 - A14	Input	Address Inputs: Provide the row address for ACTIVATE Commands and the column address for Read/Write commands to select one location out of the memory array in the respective bank. A10/AP, A12/BC_n, and WE_n/A14 have additional functions. See other rows. The address inputs also provide the op-code during Mode Register Set commands.
BA0 - BA1	Input	Bank Addresses: BA0 - BA1 define to which bank an Active, Read, Write or Precharge command is being applied. Bank address also determines which mode register is to be accessed during a MRS cycle.
A10/AP	Input	Address Input/Auto-precharge: A10 is sampled during Read/Write commands to determine whether Autoprecharge should be performed to the accessed bank after the Read/Write operation. (HIGH: Autoprecharge; LOW: no Autoprecharge). A10 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by bank addresses.
A12/BC_n	Input	Address Input/Burst chop: A12/BC_n is sampled during Read and Write commands to determine if burst chop (on-the-fly) will be performed. (HIGH, no burst chop; LOW: burst chopped). See command truth table for details.
A14/WE_n CAS _n RAS_n	Input	Command Inputs: RAS_n, CAS_n, and WE_n/A14 (along with CS_n) define the command being entered. This pin has a multi function. For example, for activation with ACT_n Low, A14 serves as an Address but for non-activation command with ACT_n High, A14 becomes a Command pin for Read, Write and other command defined in command truth table.
ACT_n	Input	Activation Command Input: ACT_n defines the Activation command being entered along with CS_n. The input into WE_n/A14 will be considered as Row Address A14.
ALERT_n	Output	Alert Output: It has multi functions such as CRC error flag , Command and Address Parity error flag as Output signal. If there is error in CRC, then ALERT_n goes LOW for the period time interval and goes back HIGH. If there is error in Command Address Parity Check, then ALERT_n goes LOW for relatively long period until on going DRAM internal recovery transaction is complete. Using this signal or not is dependent on the system. This is an open drain signal. It requires a pullup resistor on the system.
BG0 - BG1	Input	Bank Group Addresses: BG0 - BG1 define which bank group an Active, Read, Write or Precharge command is being applied. BG0 also determines which mode register is to be accessed during a MRS cycle. For x4/x8 based SDRAMs, BG0 and BG1 are valid. For x16 based SDRAM components only BG0 is valid.
CB0 - CB7	I/O	Check Bits: Used for system error detection and correction.
CK0_t, CK0_c	Input	Clock: CK_t and CK_c are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK_t and negative edge of CK_c.
CKE0	Input	Clock Enable: CKE HIGH activates and CKE LOW deactivates internal clock signals and device input buffers and output drivers. Taking CKE LOW provides Precharge Power-Down and Self-Refresh operation (all banks idle), or Active Power-Down (row Active in any bank). CKE is synchronous for Self-Refresh exit. After VREFCA and Internal DQ Vref have become stable during the power on and initialization sequence, they must be maintained during all operations (including Self-Refresh). CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK_t,CK_c, ODT and CKE, are disabled during power-down. Input buffers, excluding CKE, are disabled during Self-Refresh.

Pin Description

Symbol	Type	Description
DM_n/DBI_n	I/O	Input Data Mask and Data Bus Inversion: DM_n is an input mask signal for write data. Input data is masked when DM_n is sampled LOW coincident with that input data during a Write access. DM_n is sampled on both edges of DQS. DM is mixed with DBI function. DBI_n is an input/output identifying whether to store/output the true or inverted data. If DBI_n is LOW, the data will be stored/output after inversion inside the DDR4 SDRAM and not inverted if DBI_n is HIGH.
DQ0 - DQ63	I/O	Data Input/ Output: Bi-directional data bus. If CRC is enabled via Mode register then CRC code is added at the end of Data Burst. Any DQ from DQ0-DQ3 may indicate the internal Vref level during test via Mode Register Setting MR4 A4=High. Refer to vendor specific data sheets to determine which DQ is used.
DQS_t, DQS_c	I/O	Data Strobe: Differential data strobes. Output with read data, input with write data. Edge-aligned with read data, centered in write data. DDR4 SDRAMs support differential data strobe only and does not support single-ended.
EVENT_n	Output	Temperature Event: The #EVENT pin is asserted by the temperature sensor after it is programmed to do so. I2C thermal event indicator. Open drain, requires a pullup resistor on the system.
PARITY	Input	Parity for command and address: This function can be enabled or disabled via the mode register. When enabled in MR5, the DRAM calculates parity with ACT_n, RAS_n, CAS_n, WE_n/A14, BG[1:0], BA[1:0], A[14:0]. Input parity should be maintained at the rising edge of the clock and at the same time as command and address with CS_n LOW.
NC	-	No Connect: These pins are not connected on the module.
ODT0	Input	On-Die Termination: ODT (registered HIGH) enables RTT_NOM termination resistance internal to the DDR4 SDRAM. When enabled, ODT is only applied to each DQ, DQS_t, DQS_c and DM_n/DBI_n/, signal. The ODT pin will be ignored if MR1 is programmed to disable RTT_NOM.
RESET_n	Input (CMOS)	Active Low Asynchronous Reset: Reset is active when RESET_n is LOW, and inactive when RESET_n is HIGH. RESET_n must be HIGH during normal operation.
CS0_n	Input	Chip Select: All commands are masked when CS_n is registered HIGH. CS_n provides for external Rank selection on systems with multiple Ranks. CS_n is considered part of the command code.
SA0 - SA2	Input	Serial Address Inputs: Used to configure the temperature sensor/SPD EEPROM address range on the I^2C bus.
SCL	Input	Serial Clock Inputs: Used to synchronize communication to and from the temperature sensor/SPD EEPROM on the I^2C bus. Open drain and requires a pullup resistor on the system.
SDA	I/O	Serial Data: Used to transfer addresses and data into and out of the temperature sensor/SPD EEPROM on the I^2C bus. Open drain and requires a pullup resistor on the system.
V_{DD}	Power	Power Supply: 1.2V (Typ.) +/- 0.06 V
$V_{DD}SPD$	Power	Power Supply for SPD EEPROM with Temperature Sensor
V_{PP}	Power	DRAM Activating Power Supply: 2.5 V (2.375 V min, 2.75 V max)
$V_{REF}CA$	Power	Reference voltage for CA
V_{SS}	Power	Ground
V_{TT}	Power	Termination Voltage: Used for control, command, and address $V_{DD}/2$.

Pin Connection



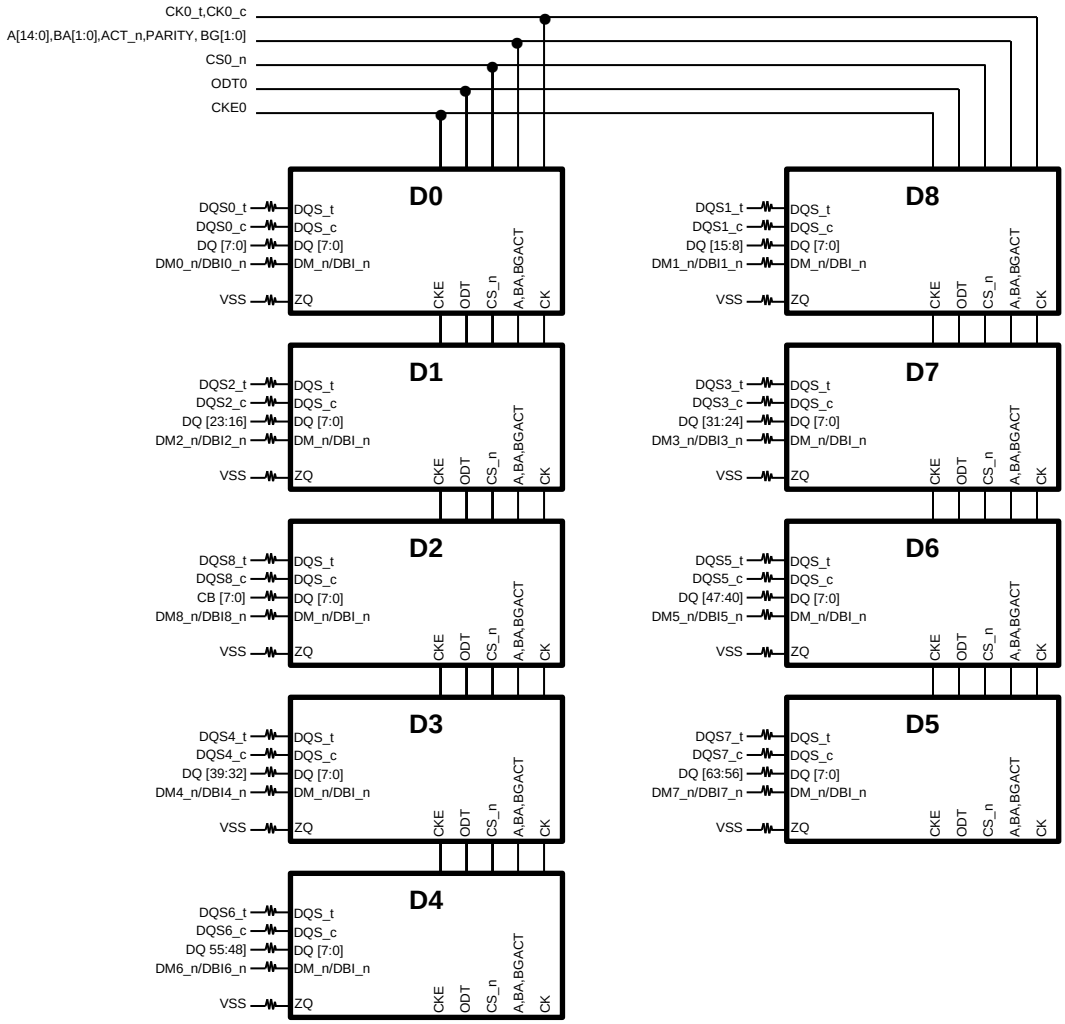
Pin Assignment

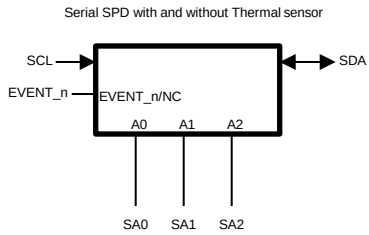
DDR4 SO-DIMM Front							
Pin#	**Pin Name**	**Pin#**	**Pin Name**	**Pin#**	**Pin Name**	**Pin#**	**Pin Name**
1	V_{SS}	67	DQ29	133	A1	197	V_{SS}
3	DQ5	69	V_{SS}	135	V_{DD}	199	DM5_n,DBI5_n
5	V_{SS}	71	DQ25	137	CK0_t	201	V_{SS}
7	DQ1	73	V_{SS}	139	CK0_c	203	DQ46
9	V_{SS}	75	DM3_n,DBI3_n	141	V_{DD}	205	V_{SS}
11	DQS0_c	77	V_{SS}	143	PARITY	207	DQ42
13	DQS0_t	79	DQ30	**Key**		209	V_{SS}
15	V_{SS}	81	V_{SS}	145	BA1	211	DQ52
17	DQ7	83	DQ26	147	V_{DD}	213	V_{SS}
19	V_{SS}	85	V_{SS}	149	CS0_n	215	DQ49
21	DQ3	87	CB5	151	A14/WE_n	217	V_{SS}
23	V_{SS}	89	V_{SS}	153	V_{DD}	219	DQS6_c
25	DQ13	91	CB1	155	ODT0	221	DQS6_t
27	V_{SS}	93	V_{SS}	157	NC	223	V_{SS}
29	DQ9	95	DQS8_c	159	V_{DD}	225	DQ55
31	V_{SS}	97	DQS8_t	161	NC	227	V_{SS}
33	DM1_n,DBI1_n	99	V_{SS}	163	V_{DD}	229	DQ51
35	V_{SS}	101	CB2	165	NC	231	V_{SS}
37	DQ15	103	V_{SS}	167	V_{SS}	233	DQ61
39	V_{SS}	105	CB3	169	DQ37	235	V_{SS}
41	DQ10	107	V_{SS}	171	V_{SS}	237	DQ56
43	V_{SS}	109	CKE0	173	DQ33	239	V_{SS}
45	DQ21	111	V_{DD}	175	V_{SS}	241	DM7_n,DBI7_n
47	V_{SS}	113	BG1	177	DQS4_c	243	V_{SS}
49	DQ17	115	BG0	179	DQS4_t	245	DQ62
51	V_{SS}	117	V_{DD}	181	V_{SS}	247	V_{SS}
53	DQS2_c	119	A12/BC_n	183	DQ38	249	DQ58
55	DQS2_t	121	A9	185	V_{SS}	251	V_{SS}
57	V_{SS}	123	V_{DD}	187	DQ34	253	SCL
59	DQ23	125	A8	189	V_{SS}	255	V_{DD}SPD
61	V_{SS}	127	A6	191	DQ44	257	V_{PP}
63	DQ19	129	V_{DD}	193	V_{SS}	259	V_{PP}
65	V_{SS}	131	A3	195	DQ40		

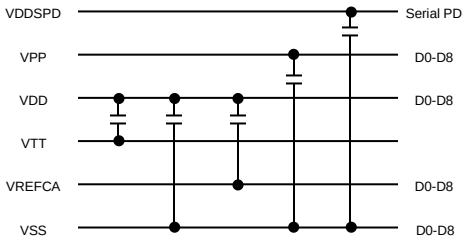
Pin Assignment

DDR4 SO-DIMM Back							
Pin#	**Pin Name**	**Pin#**	**Pin Name**	**Pin#**	**Pin Name**	**Pin#**	**Pin Name**
2	V_{SS}	68	V_{SS}	134	EVENT_n	198	DQS5_c
4	DQ4	70	DQ24	136	V_{DD}	200	DQS5_t
6	V_{SS}	72	V_{SS}	138	NC	202	V_{SS}
8	DQ0	74	DQS3_c	140	NC	204	DQ47
10	V_{SS}	76	DQS3_t	142	V_{DD}	206	V_{SS}
12	DM0_n,DBI0_n	78	V_{SS}	144	A0	208	DQ43
14	V_{SS}	80	DQ31	**Key**		210	V_{SS}
16	DQ6	82	V_{SS}	146	A10/AP	212	DQ53
18	V_{SS}	84	DQ27	148	V_{DD}	214	V_{SS}
20	DQ2	86	V_{SS}	150	BA0	216	DQ48
22	V_{SS}	88	CB4	152	RAS_n	218	V_{SS}
24	DQ12	90	V_{SS}	154	V_{DD}	220	DM6_n,DBI6_n
26	V_{SS}	92	CB0	156	CAS_n	222	V_{SS}
28	DQ8	94	V_{SS}	158	A13	224	DQ54
30	V_{SS}	96	DM8_n,DBI8_n	160	V_{DD}	226	V_{SS}
32	DQS1_c	98	V_{SS}	162	CNC	228	DQ50
34	DQS1_t	100	CB6	164	$V_{REF}CA$	230	V_{SS}
36	V_{SS}	102	V_{SS}	166	SA2	232	DQ60
38	DQ14	104	CB7	168	V_{SS}	234	V_{SS}
40	V_{SS}	106	V_{SS}	170	DQ36	236	DQ57
42	DQ11	108	RESET_n	172	V_{SS}	238	V_{SS}
44	V_{SS}	110	NC	174	DQ32	240	DQS7_c
46	DQ20	112	V_{DD}	176	V_{SS}	242	DQS7_t
48	V_{SS}	114	ACT_n	178	DM4_n,DBI4_n	244	V_{SS}
50	DQ16	116	ALERT_n	180	V_{SS}	246	DQ63
52	V_{SS}	118	V_{DD}	182	DQ39	248	V_{SS}
54	DM2_n,DBI2_n	120	A11	184	V_{SS}	250	DQ59
56	V_{SS}	122	A7	186	DQ35	252	V_{SS}
58	DQ22	124	V_{DD}	188	V_{SS}	254	SDA
60	V_{SS}	126	A5	190	DQ45	256	SA0
62	DQ18	128	A4	192	V_{SS}	258	V_{TT}
64	V_{SS}	130	V_{DD}	194	DQ41	260	SA1
66	DQ28	132	A2	196	V_{SS}		

Block Diagram







Note 1. Unless otherwise noted, resistor values are 15Ω ±5%.
Note 2. ZQ Resistors are 240Ω ±1%. For all other resistor values refer to the appropriate writing diagram.

Absolute Maximum DC Ratings

Symbol	Parameter	MIN	MAX	Units	Note
VDD	VDD supply voltage relative to VSS	-0.3	1.5	V	1,3
VDDQ	VDDQ supply voltage relative to VSS	-0.3	1.5	V	1,3
VPP	Voltage on VPP pin relative to VSS	-0.3	3	V	4
V_{IN}, V_{OUT}	Voltage on any pin relative to VSS	-0.3	1.5	V	1,3,5
T_{STG}	Storage Temperature	-55	100	°C	1,2

Notes:
1. Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.
3. VDD and VDDQ must be within 300mV of each other at all times; and VREFCA must be not greater than 0.6 x VDDQ, When VDD and VDDQ are less than 500 mV; VREF may be equal to or less than 300 mV.
4. VPP must be equal or greater than VDD/VDDQ at all times.
5. Overshoot area above 1.5V is specified in DDR4 Device Operation.

DRAM Component Operating Temperature Range

Symbol	Parameter	Rating	Units	Note
TOPER	Normal Temperature Range	0 to 85	°C	1,2
	Extended Temperature Range (optional)	85 to 95	°C	1,3

Notes:
1. Operating Temperature TOPER is the case surface temperature on the center / top of the DRAM. For measurement conditions, please refer to the JEDEC document JESD51-2.
2. The Normal Temperature Range specifies the temperatures where all DRAM specifications will be supported. During operation, the DRAM case temperature must be maintained between 0˚ C to +85˚ C under all operating conditions.
3. Some applications require operation of the DRAM in the Extended Temperature Range between +85˚ C to +95˚ C case temperature. Full specifications are guaranteed in this range, but the following additional conditions apply:
    1. Refresh commands must be doubled in frequency, therefore reducing the Refresh interval tREFI to 3.9 µs. It is also possible to specify a component with 1X refresh (tREFI to 7.8µs) in the Extended Temperature Range. Please refer to the DIMM SPD for option availability.
    2. If Self-Refresh operation is required in the Extended Temperature Range, then it is mandatory to either use the Manual Self-Refresh mode with Extended Temperature Range capability (MR2 A6 = 0b and MR2 A7 = 1b) or enable the optional Auto Self-Refresh mode (MR2 A6 = 1b and MR2 A7 = 0b). DDR4 SDRAMs support Auto Self-Refresh and in Extended Temperature Range and please refer to component datasheet and/or the DIMM SPD for tREFI requirements in the Extended Temperature Range.

Operating Conditions

Symbol	Parameter	MIN	Nom	MAX	Units	Note
VDD	VDD supply voltage	1.14	1.2	1.26	V	1
VDDQ	VDDQ supply voltage	1.14	1.2	1.26	V	1
VPP	DRAM activating power supply	2.375	2.5	2.75	V	2

Notes:
1. Under all conditions VDDQ must be less than or equal to VDD.
2. VDDQ tracks with VDD. AC parameters are measured with VDD and VDDQ tied together.
3. DC bandwidth is limited to 20MHz.

DC Characteristics

(TC = 0° C to +85° C, VDD = 1.2V ± 0.06V, VSS = 0V)

Parameter	Symbol	MAX	Unit
ACTIVE-PRECHARGE Current	IDD0	324	mA
ACTIVE-PRECHARGE, Word Line Boost, IPP current	IPP0	27	mA
ACTIVE-READ-PRECHARGE Current	IDD1	360	mA
Precharge standby Current	IDD2N	180	mA
Precharge standby ODT Current	IDD2NT	198	mA
Precharge Power-Down Current CKE	IDD2P	117	mA
Precharge quiet standby current	IDD2Q	162	mA
Active standby Current	IDD3N	297	mA
Active standby IPP current	IPP3N	18	mA
Active Power-Down Current	IDD3P	162	mA
Operating Burst Read Current	IDD4R	999	mA
Operating Burst Write Current	IDD4W	936	mA
Burst Refresh Current	IDD5B	1773	mA
Burst refresh IPP current (1x REF)	IPP5B	189	mA
Self Refresh Current : Normal Temperature Range	IDD6N	171	mA
Self Refresh Current : Extended Temperature Range	IDD6E	180	mA
Self Refresh Current : Reduced Temperature Range	IDD6R	171	mA
Auto Self Refresh Current	IDD6A	171	mA
Bank Interleave Read Current	IDD7	1386	mA
Bank Interleave Read IPP Current	IPP7	99	mA
Maximum Power Down Current	IDD8	54	mA

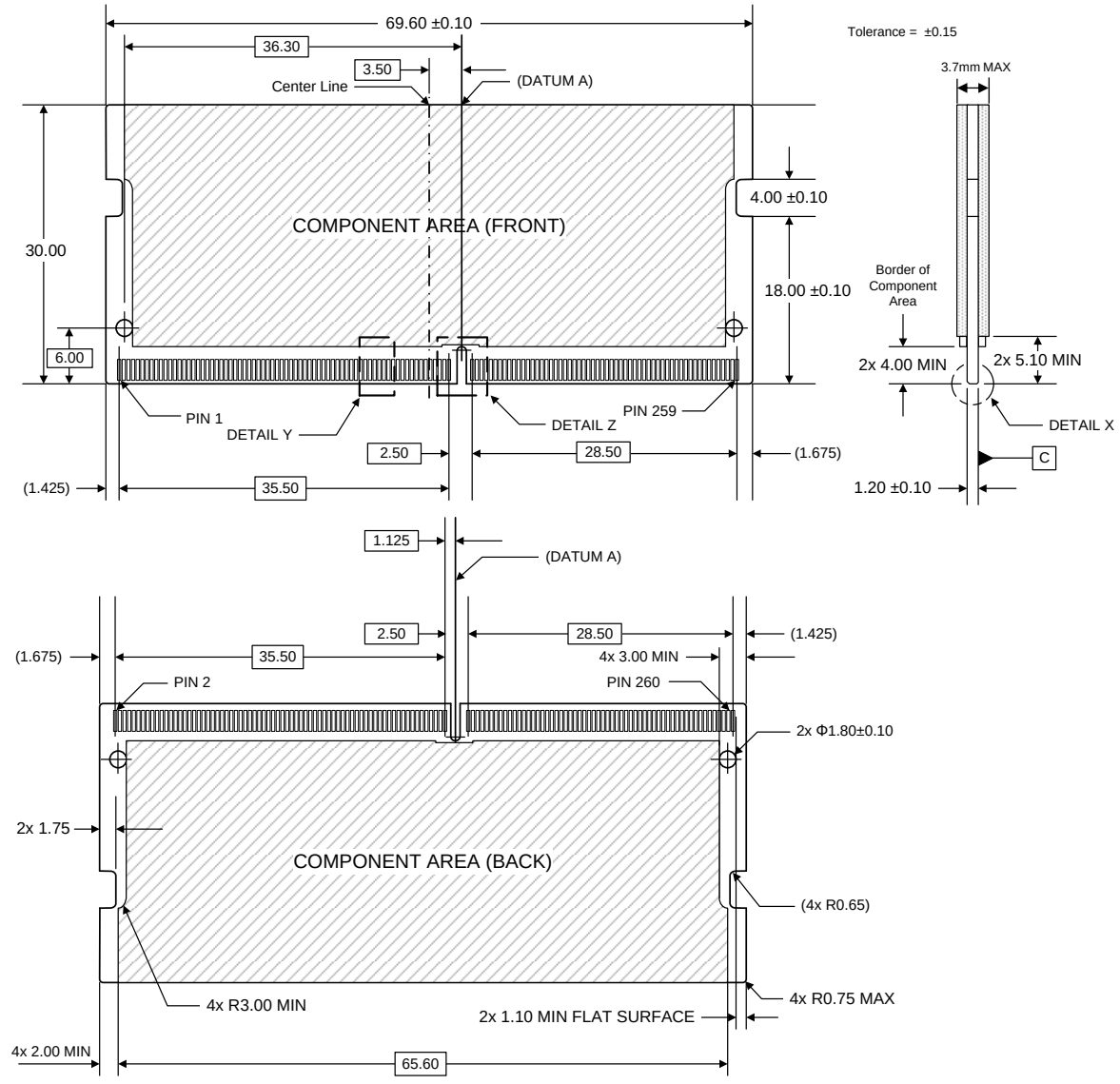
Serial Presence Detect

Byte	Byte Description	Notes	Value(Hex)
0	Number of Bytes Used / Number of Bytes in SPD device	384Bytes, 512Bytes	23
1	SPD Revision	Rev. 1.2	12
2	Key Byte / DRAM Device Type	DDR4 SDRAM	0C
3	Key Byte / Module type	72b-SO-UDIMM	09
4	SDRAM Density and Banks	2 BG, 2 BA, 4Gb	84
5	SDRAM Addressing (Row / Column)	Row 15, Col. 10	19
6	Primary SDRAM Package Type	Monolithic DRAM Device, Single Die	00
7	SDRAM Optional Features	8192 x tREFI, Unlimited MAC	08
8	SDRAM Thermal and Refresh Options	-	00
9	Other SDRAM Optional Features	Post package repair supported, Soft PPR supported	60
10	Secondary SDRAM Package Type	-	00
11	Module Nominal Voltage, VDD	Module Nominal Voltage, VDD = 1.2V	03
12	Module Organization	1 Package Rank, x8 Device	01
13	Module Memory Bus Width	64bits Primary bus + 8bits ECC	0B
14	Module Thermal Sensor	Thermal sensor is supported.	80
15	Extended Module Type	-	00
16	Reserved	-	00
17	Timebases	MTB = 125ps & FTB = 1ps	00
18	SDRAM Minimum Cycle Time (tCKAVG_min)	0.625ns (DDR4-3200)	05
19	SDRAM Maximum Cycle Time (tCKAVG_max)	1.6ns - Monolythic	0D
20	CAS Latencies Supported, First Byte	CL = 14, 13, 12, 11, 10	F8
21	CAS Latencies Supported, Second Byte	CL = 22, 21, 20, 19, 18, 17, 16, 15	FF
22	CAS Latencies Supported, Third Byte	CL = 28, 26, 25, 24, 23	2F
23	CAS Latencies Supported, Fourth Byte	-	00
24	Minimum CAS Latency Time (tAA_min)	13.75ns	6E
25	Minimum RAS to CAS Delay Time (tRCD_min)	13.75ns	6E
26	Minimum Row Precharge Delay Time (tRP_min)	13.75ns	6E
27	Upper Nibbles for tRAS_min and tRC_min	-	11
28	Minimum Active to Precharge Delay Time (tRAS_min), Least Significant Byte	32ns	00
29	Minimum Active to Active / Refresh Delay Time (tRC_min), Least Significant Byte	45.75ns	6E
30	Minimum Refresh Recovery Delay Time (tRFC1_min), Least Significant Byte	260ns	20
31	Minimum Refresh Recovery Delay Time (tRFC1_min), Most Significant Byte		08
32	Minimum Refresh Recovery Delay Time (tRFC2_min), Least Significant Byte	160ns	00
33	Minimum Refresh Recovery Delay Time (tRFC2_min), Most Significant Byte		05
34	Minimum Refresh Recovery Delay Time (tRFC4_min), Least Significant Byte	110ns	70
35	Minimum Refresh Recovery Delay Time (tRFC4_min), Most Significant Byte		03
36	Upper Nibble for tFAW	21ns	00
37	Minimum Four Activate Window Delay Time (tFAW_min), Least Significant Byte		A8
38	Minimum Activate to Activate Delay Time (tRRD_S_min), Different Bank Group	2.5ns	14
39	Minimum Activate to Activate Delay Time (tRRD_L_min), Same Bank Group	4.9ns	28
40	Minimum CAS to CAS Delay Time (tCCD_L_min), Same Bank Group	5ns	28
41	Upper Nibble for tWR_min	15ns	00
42	Minimum Write Recovery Time (tWR_min)		78
43	Upper Nibble for tWTR_min	-	00
44	Minimum Write to Read Time (tWTR_S_min), Different Bank Group	2.5ns	14
45	Minimum Write to Read Time (tWTR_L_min), Same Bank Group	7.5ns	3C
46 - 59	Reserved	-	00
60	Connector to SDRAM Bit Mapping: DQ 0-3	SDRAM Bit order = 1, 3, 2, 0	0C
61	Connector to SDRAM Bit Mapping: DQ 4-7	SDRAM Bit order = 5, 7, 4, 6	2B
62	Connector to SDRAM Bit Mapping: DQ 8-11	SDRAM Bit order = 6, 4, 5, 7	2D
63	Connector to SDRAM Bit Mapping: DQ 12-15	SDRAM Bit order = 0, 2, 3, 1	04
64	Connector to SDRAM Bit Mapping: DQ 16-19	SDRAM Bit order = 3, 1, 2, 0	16
65	Connector to SDRAM Bit Mapping: DQ 20-23	SDRAM Bit order = 7, 5, 4, 6	35
66	Connector to SDRAM Bit Mapping: DQ 24-27	SDRAM Bit order = 4, 6, 5, 7	23
67	Connector to SDRAM Bit Mapping: DQ 28-31	SDRAM Bit order = 2, 0, 1, 3	0D
68	Connector to SDRAM Bit Mapping: CB 0-3	SDRAM Bit order = 7, 5, 6, 4	36
69	Connector to SDRAM Bit Mapping: CB 4-7	SDRAM Bit order = 1, 3, 2, 0	0C
70	Connector to SDRAM Bit Mapping: DQ 32-35	SDRAM Bit order = 5, 7, 6, 4	2C
71	Connector to SDRAM Bit Mapping: DQ 36-39	SDRAM Bit order = 1, 3, 0, 2	0B
72	Connector to SDRAM Bit Mapping: DQ 40-43	SDRAM Bit order = 0, 2, 1, 3	03
73	Connector to SDRAM Bit Mapping: DQ 44-47	SDRAM Bit order = 4, 6, 7, 5	24
74	Connector to SDRAM Bit Mapping: DQ 48-51	SDRAM Bit order = 7, 5, 4, 6	35
75	Connector to SDRAM Bit Mapping: DQ 52-55	SDRAM Bit order = 1, 3, 2, 0	0C
76	Connector to SDRAM Bit Mapping: DQ 56-59	SDRAM Bit order = 0, 2, 1, 3	03
77	Connector to SDRAM Bit Mapping: DQ 60-63	SDRAM Bit order = 6, 4, 5, 7	2D

Serial Presence Detect

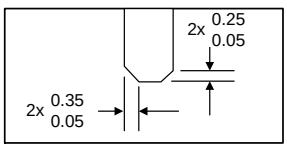
Byte	Byte Description	Notes	Value(Hex)
78 - 116	Reserved	-	00
117	Fine Offset for Minimum CAS to CAS Delay Time (tCCD_L_min), Same Bank Group	0ps	00
118	Fine Offset for Minimum Activate to Activate Delay Time (tRRD_L_min), Same Bank Group	-0.100ns	9C
119	Fine Offset for Minimum Activate to Activate Delay Time (tRRD_S_min), Different Bank Group	0ps	00
120	Fine Offset for Minimum Active to Active / Refresh Delay Time (tRC_min)	0ps	00
121	Fine Offset for Minimum Row Precharge Delay Time (tRP_min)	0ps	00
122	Fine Offset for Minimum RAS to CAS Delay Time (tRCD_min)	0ps	00
123	Fine Offset for Minimum CAS Latency Time (tAA_min)	0ps	00
124	Fine Offset for SDRAM Maximum Cycle Time (tCKAVG_max)	-0.025ns	E7
125	Fine Offset for SDRAM Minimum Cycle Time (tCKAVG_min)	0ps	00
126	Cyclical Redundancy Code (CRC) for Base Configuration Section, LSB		15
127	Cyclical Redundancy Code (CRC) for Base Configuration Section, MSB		4D
128	Raw Card Extension, Module Nominal Height	29 < Height ≦ 30mm	0F
129	Module Maximum Thickness	1 < Front ≦ 2mm / 1 < Back ≦ 2mm	11
130	Reference Raw Card Used	Raw Card D Rev. 2	43
131	Address Mapping from Edge Connector to DRAM	No Rank 1	00
132 - 191	Reserved	-	00
192 - 253	Reserved	-	00
254	Cyclical Redundancy Code (CRC) for SPD Block 1, LSB		61
255	Cyclical Redundancy Code (CRC) for SPD Block 1, MSB		BB
256 - 319	Reserved	-	00
320	Module Manufacturer ID code, LSB	ADTEC Corporation	02
321	Module Manufacturer ID code, MSB		29
322	Module Manufacturing Location	Japan	01
323	Module Manufacturing Date	(e.g.)Year2024	24
324	Module Manufacturing Date	(e.g.)Week01	01
325	Module Serial Number	(e.g.)S/N: 00000000	00
326	Module Serial Number		00
327	Module Serial Number		00
328	Module Serial Number		00
329	Module Part Number	3	33
330	Module Part Number	2	32
331	Module Part Number	0	30
332	Module Part Number	0	30
333	Module Part Number	T	54
334	Module Part Number	0	30
335	Module Part Number	4	34
336	Module Part Number	G	47
337	Module Part Number	1	31
338	Module Part Number	8	38
339	Module Part Number	4	34
340	Module Part Number	S	53
341	Module Part Number	G	47
342	Module Part Number	-	20
343	Module Part Number	-	20
344	Module Part Number	-	20
345	Module Part Number	-	20
346	Module Part Number	-	20
347	Module Part Number	-	20
348	Module Part Number	-	20
349	Module Revision Code	1st Revision	01
350	DRAM Manufacturer ID Code, LSB	Samsung	80
351	DRAM Manufacturer ID Code, MSB		CE
352	DRAM Stepping	G-die	47
353 - 381	Manufacturer's Specific Data	-	00
382 - 383	Reserved	-	00
384 - 512	Reserved	-	00

Outline Dimensions

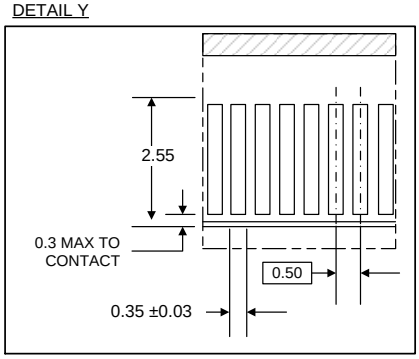


[#] : BASIC
(#) : REFERENCE

DETAIL X



DETAIL Y



DETAIL Z